

BCM97630REF2A [P1]

824-118834-0000

REV	DATE	BY	ECO#	SHEET	DESCRIPTION
P1	2009-09-30	JZ	BCG-06475	-	Initial Release

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Memory Populated On 100-118834-0000

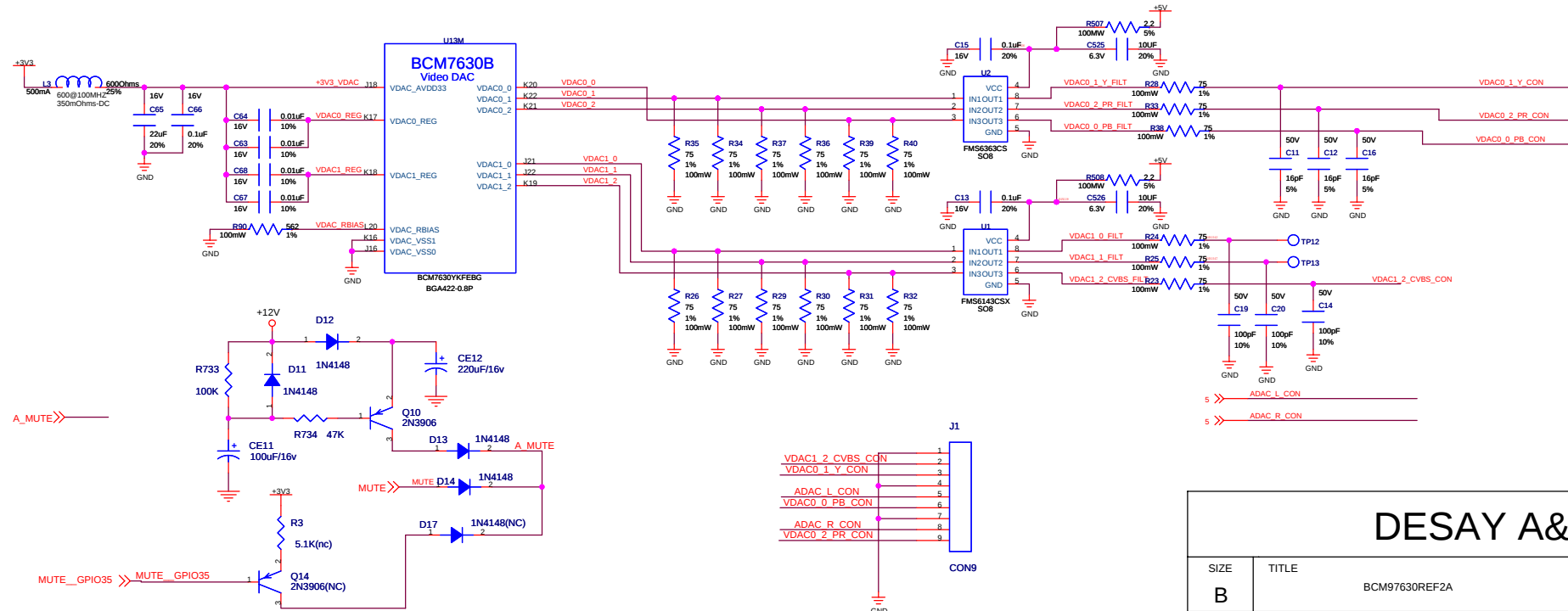
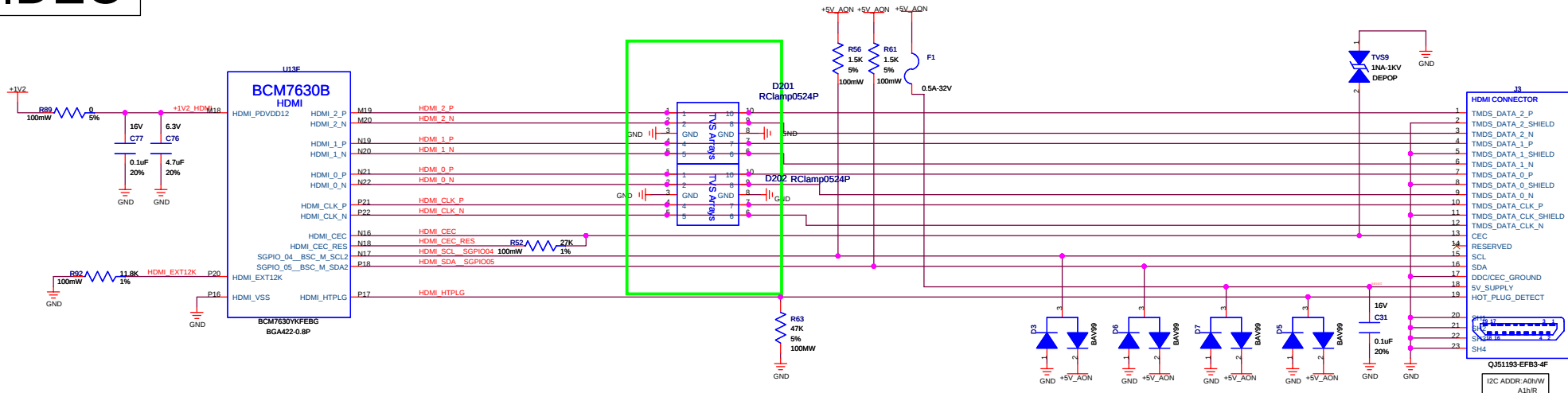
NAND	538231-00 2Gbit (256MX8)TOSOP48 NUMONIX NAND02GW3B2DN6E
DDR3	540727-00 1Gbit (64MX16) 1.5V DDR3-1333 FBGA96 SAMSUNG K4B1G1646E-HCH9
3 Device 384MBytes	540726-00 1Gbit (128MX8) 1.5V DDR3-1333 FBGA78 SAMSUNG K4B1G0846E-HCH9
	540726-00 1Gbit (128MX8) 1.5V DDR3-1333 FBGA78 SAMSUNG K4B1G0846E-HCH9

DESAY A&V SCIENCE AND TECHNOLOGY CO.,LTD		
Company Confidential		
SIZE B	TITLE BCM97630+SANYO OPU	
Designer		Drawing Number Version 0.1
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DESAY A&V

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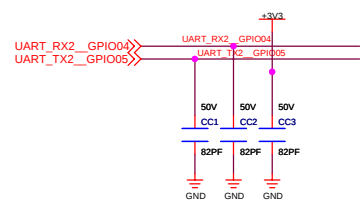
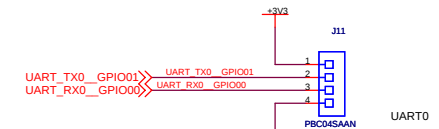
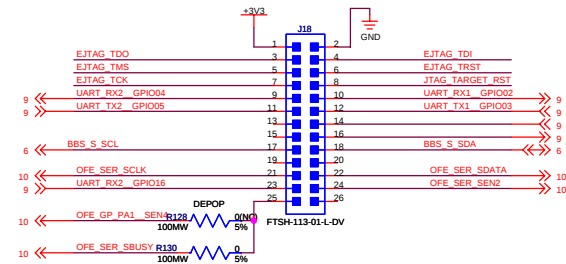
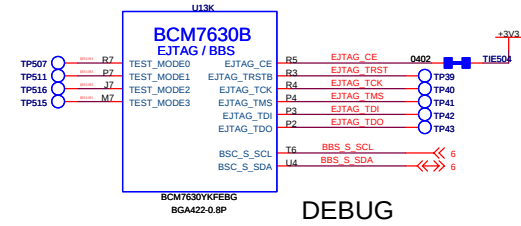
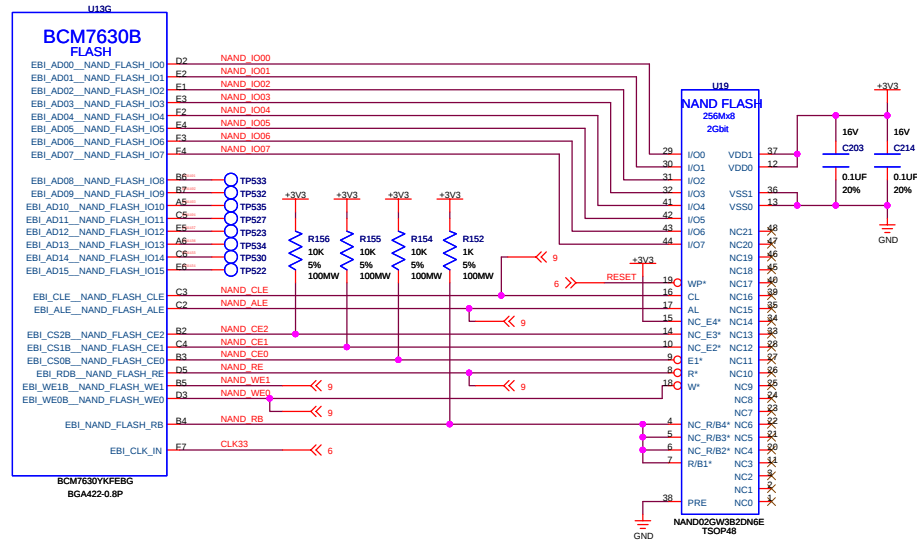
VIDEO



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SIZE	TITLE
B	BCM97630REF2A
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SHEET	4 OF 12

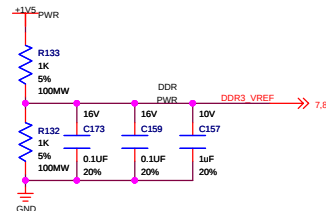
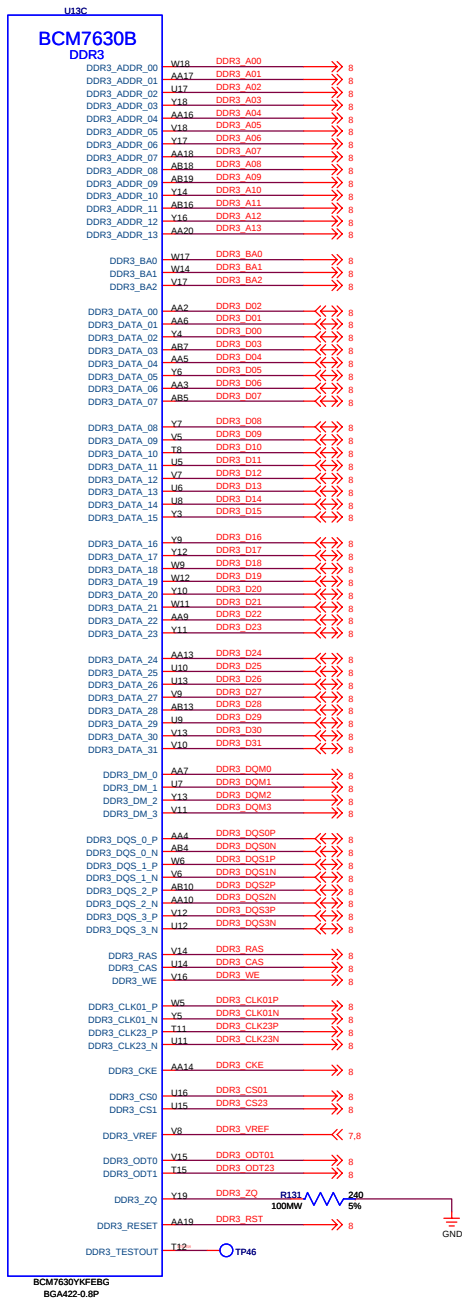
NAND, Clock, Test, Reset, 2.5V



DESAY A&V

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DDR3



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DDR3 parts

U21
DDR3
64M x 16 (1Gbit)
FBGA 96

U14A1
DDR3
128M x 8 (1Gbit)
FBGA 78

U14B1
DDR3
128M x 8 (1Gbit)
FBGA 78

DESAY A&V

SIZE
B

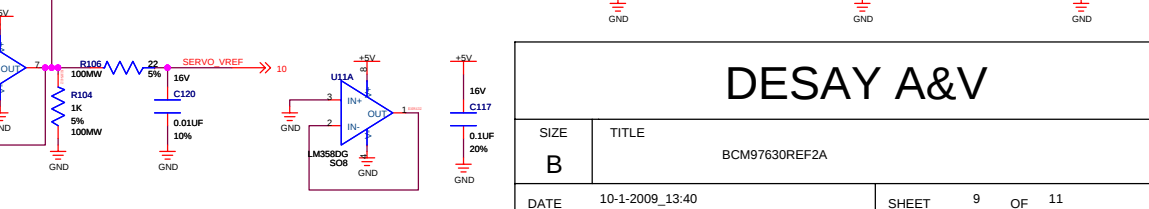
TITLE
BCM97630REF2A

DATE
10-1-2009_13:40

SHEET
7

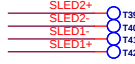
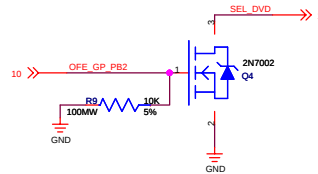
OF
11

A



DATE	10-1-2009_13:40	SHEET	9	OF	11
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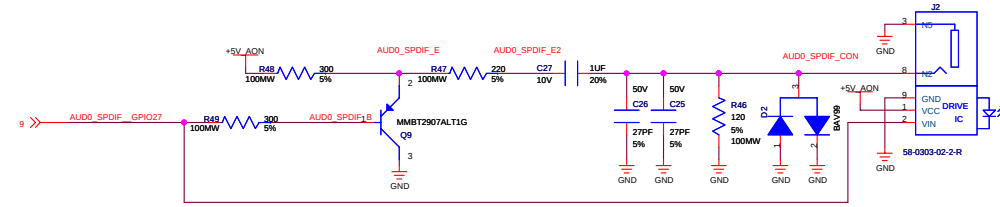
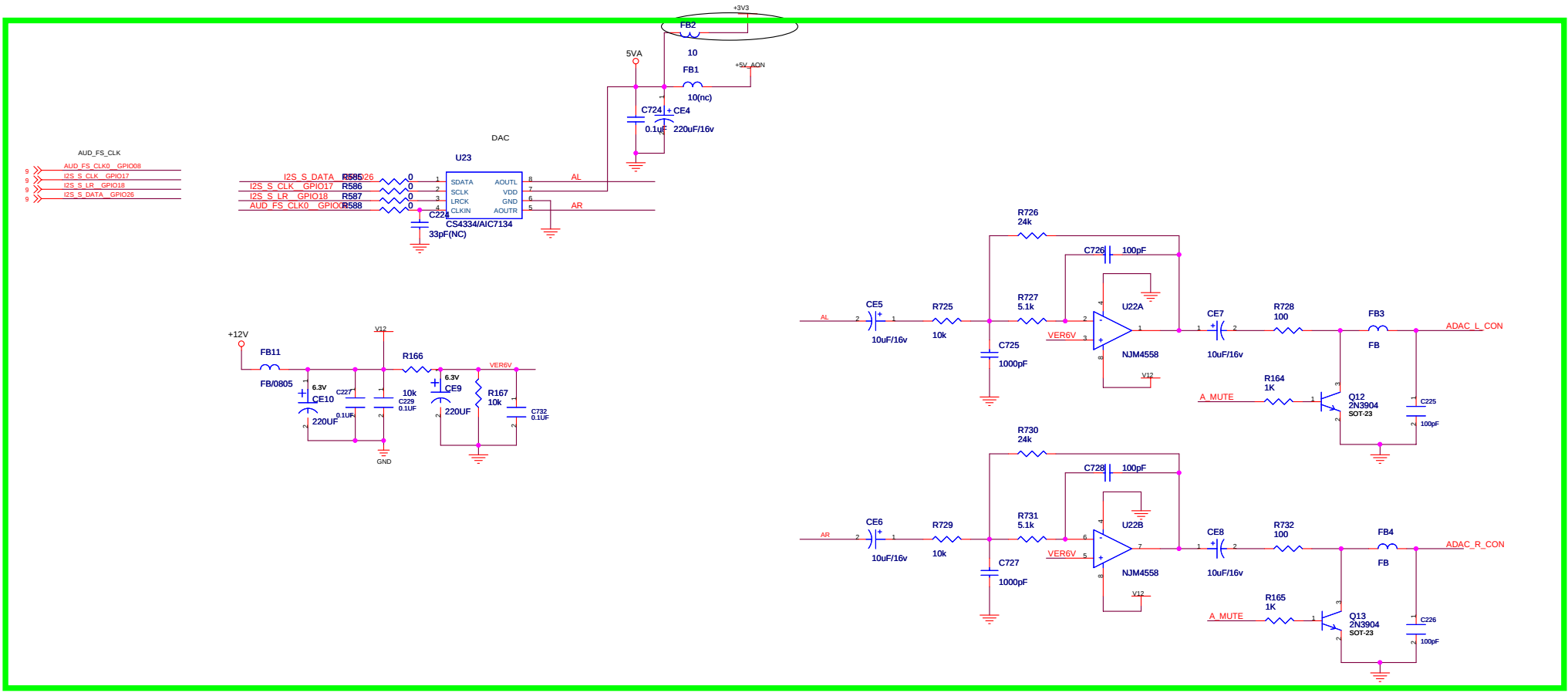
A



1	GND	
2	GND	
3	EJECT#	
4	CLOSE#	
5	LOAD-	DOOR
6	OPEN#	
7	LOAD+	
8	GND	
9	U COIL	SPINDLE
10	V COIL	
11	W COIL	
12	COM	
13	GND	
14	SLED2+	SLED
15	SLED2-	
16	SLED1-	
17	SLED1+	
18	GND	

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AUDIO



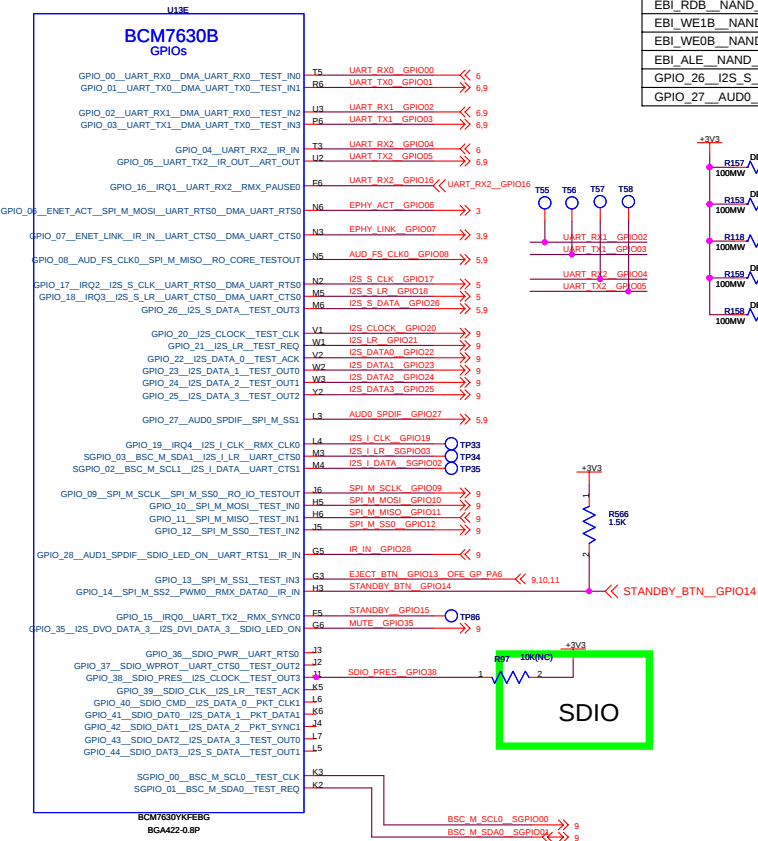
ADAC_L_CON
ADAC_R_CON
A_MUTE

<OrigName>		
Size	Document Number	Rev
Custom	<Doc>	<RevCode>
Date	Saturday, February 27, 2010	Sheet 1 of 1

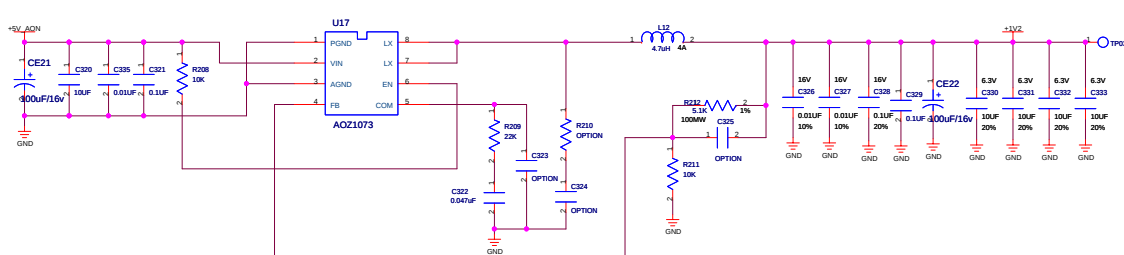
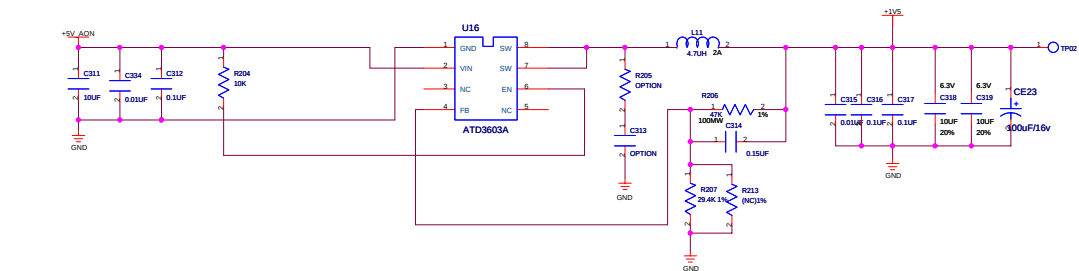
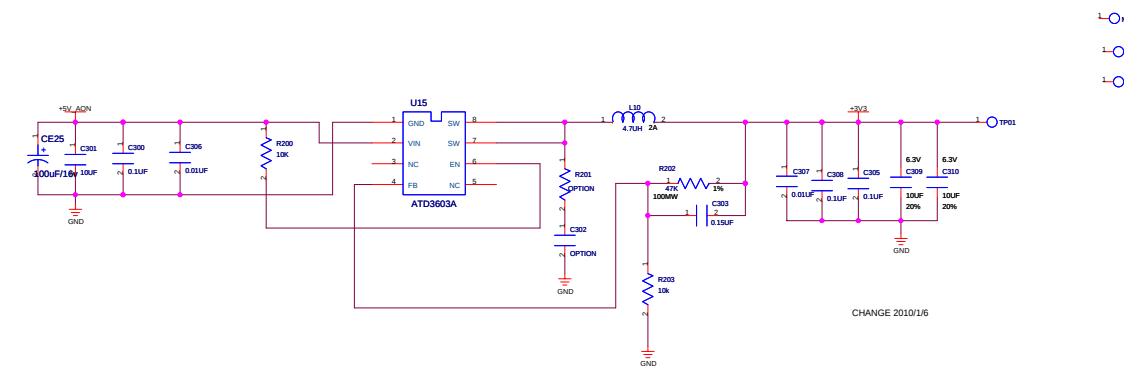
GPIO

Boot Strap Options

Signal / Pin	Strap Name	Description	Value
EBI_CLE_NAND_FLASH_CLE	STRAP_NAND_FLASH_TYPE3	15 = One NAND 5 = 12 Bit ECC 4 = 8 Bit ECC (27 Bit OBB)	2
EBI_RDB_NAND_FLASH_RE	STRAP_NAND_FLASH_TYPE2	3 = 8 Bit ECC (16 Bit OBB) 2 = 4 Bit ECC 1 = 1 Bit ECC 0 = No ECC	
EBI_WE1B_NAND_FLASH_WE1	STRAP_NAND_FLASH_TYPE1		
EBI_WE0B_NAND_FLASH_WE0	STRAP_NAND_FLASH_TYPE0		
EBI_ALE_NAND_FLASH_ALE	STRAP_TEST_ENABLE	0 = Little endian, 1 = Big endian	
GPIO_26_I2S_S_DATA_TEST_OUT	STRAP_SYSTEM_BIG_ENDIAN	1 = Extend initial Reset	
GPIO_27_AUD0_SPDIF_SPI_M_SSI	STRAP_RESET_EXT_MODE	0 = Normal, 1 = Disable MIPS Boot	

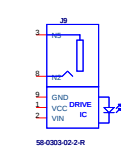
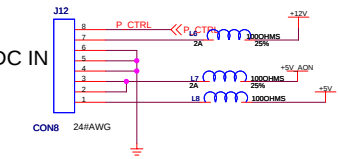


Power



- M1
- M2
- M3

DC_CON



CHANGE 2010/1/6

